AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1-10. (canceled)

11. (original) An integrated circuit comprising:

a logic circuit developing first and second input signals complementary to each other, wherein said logic circuit includes:

a first pull-up N-channel MISFET used for pull-up of said first input signal, and

a second pull-up N-channel MISFET used for pull-up of said second input signal; and

a differential output circuit including:

a first input receiving said first input signal;

a second input receiving said second input signal;

first and second outputs;

a resistor element connected between said first and second outputs;

a first N-channel MISFET having a source connected to said first input, a gate receiving a power supply potential, and a drain connected to said first output;

a second N-channel MISFET having a source connected to said second input, a gate receiving said power supply potential, and a drain connected to said second output;

a first P-channel MISFET having a source receiving said power supply potential, a gate connected to said second input, and a drain connected to said first output; and

a second P-channel MISFET having a source receiving said power supply potential, a gate connected to said first input, and a drain connected to said second output.

12. (original) The integrated circuit according to claim 11, further comprising an inductive element, wherein said resistive element and said inductive element are connected in series between said first and second outputs.

13. (original) An integrated circuit comprising:

a logic circuit developing first and second input signals complementary to each other, wherein said logic circuit includes:

a first pull-up N-channel MISFET used for pull-up of said first input signal, and

a second pull-up N-channel MISFET used for pull-up of said second input signal; and

a differential output circuit including:

a first input receiving said first input signal;

a second input receiving said second input signal;

first and second outputs;

an inductive element connected between said first and second outputs;

a first N-channel MISFET having a source connected to said first input, a gate receiving a power supply potential, and a drain connected to said first output;

a second N-channel MISFET having a source connected to said second input, a gate receiving said power supply potential, and a drain connected to said second output;

a first P-channel MISFET having a source receiving said power supply potential, a gate connected to said second input, and a drain connected to said first output; and

a second P-channel MISFET having a source receiving said power supply potential, a gate connected to said first input, and a drain connected to said second output.